forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

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introducing N atoms, after said step of introducing said impurity element, into said gate oxide film while using said gate electrode pattern as a mask, such that said N atoms do not reach said substrate,

wherein said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions conducted under an acceleration voltage not exceeding 10keV, with a dose of $1 - 3 \times 10^{14}cm^{-2}$.